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09/816480
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Subclass	ISSUE CLASSIFICATION
Class	

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PATENT NUMBER

JC5-555

U.S. UTILITY PATENT APPLICATION

O.I.P.E.	PATENT DATE
RC 2 SCANNED SA Q.A. A.G.	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/816480	F	703	22	2123	SERGENT CHANG

APPLICANTS: Kazuyoshi Kohno
Atsushi Mizuno

TITLE: Design verification method, design verification device for microprocessors, and pipeline simulator generation device

PTO-2040
12/99

PREPARED AND APPROVED FOR ISSUE

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
INTERNATIONAL CLASSIFICATION			
			☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ a) The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) _____ (Date)			NOTICE OF ALLOWANCE MAILED	
☐ b) The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____	_____ (Primary Examiner) _____ (Date)			ISSUE FEE	
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